IN THE CLAIMS

1. (Previously presented) A data processing apparatus, the apparatus comprising an instruction address generation circuit for outputting an instruction address; an instruction memory system arranged to output an instruction word addressed by the instruction address; an instruction execution unit, arranged to process a plurality of instructions from the instruction word in parallel; a detection unit, arranged to detect in which of a plurality of ranges the instruction address lies, the detection unit being coupled to the instruction execution unit and/or the instruction memory system, to control a way in which the instruction execution unit parallelizes processing of the instructions from the instruction word, dependent on a detected range.

2. (Previously presented) A data processing apparatus according to claim 1, wherein the instruction execution unit and/or the instruction memory system is arranged to adjust a width of the instruction word that determines a number of instructions from the instruction word that is processed in parallel, dependent on the detected range.

3. (Previously presented) A data processing apparatus according to claim 1, wherein the instruction execution unit comprises a plurality of functional units, the instruction execution unit being arranged to select a subset of the functional units that is available for processing the instructions, dependent on the detected range.

4. (Previously presented) A data processing apparatus according to claim 1, wherein the instruction execution unit comprises a plurality of functional units, the instruction execution unit being arranged to select whether functional units or groups of functional units from a set of functional units each receive respective instructions from the instruction word, or receive a shared instruction from the instruction word, dependent on the detected range.

5. (Previously presented) A data processing apparatus according to claim 2, wherein the instruction memory comprises a first memory unit and a second memory unit, providing

storage with a first and second unit of width of addressable memory locations for instruction words of different lengths with addresses in a first and second range respectively, the first and second unit of width being mutually different.

6. (Currently amended) A data processing apparatus according to claim 5, programmed to execute a program, ~~relatively~~ longer instruction words from an inner loop of the program being stored in the first memory unit, ~~relatively~~ shorter instruction words from a majority of the program outside the inner loop being stored in the second memory unit, the first unit of width being larger than the second unit of width.

7. (Previously presented) A data processing apparatus according to claim 5, comprising a memory mapping unit arranged to map the instruction address onto the first memory unit or the second memory unit, dependent on the detected range.

8. (Previously presented) A data processing apparatus according to claim 5, wherein the instruction memory system is arranged to disable supply of clock signals to the first memory unit when addresses in the second range are detected.

9. (Previously presented) A data processing apparatus according to claim 5, wherein the instruction memory system is arranged to disable supply of clock signals to all but the memory unit from whose address range addresses are detected.

10. (Previously presented) A data processing apparatus according to claim 2, wherein the instruction memory system comprises a plurality of memory units, each arranged to be responsive to instruction addresses in a respective range, the instruction memory allowing partial overlap of the respective ranges, the instruction memory system being arranged to supply the instruction word as a combination of instructions from those of the memory units in whose respective range the instruction address lies.

11. (Previously presented) A data processing apparatus according to claim 10, wherein the instruction memory system is arranged to disable supply of clock signals to at least

one of the memory units when the instruction address is not in the respective range of said at least one of the memory units.

12. (Previously presented) A data processing apparatus according to claim 10, wherein the execution unit comprises groups of one or more functional units, each group being coupled to a respective predetermined one of the memory units, for receiving instructions from the instruction words, when the instruction address is in the respective range of the respective predetermined one of the memory unit to which the group is coupled.

13. (Canceled)

14. (Previously presented) A method of programming a data processing apparatus according to claim 1, the method comprising generating a program of machine instructions for the apparatus; identifying an inner loop of the program; loading the program into the instruction memory system, so that instructions from the inner loop are loaded at memory locations with instruction addresses in a range of addresses for which the apparatus provides a higher degree of parallelism than another range of addresses.

15. (Previously presented) A method of executing a program with a data processing apparatus, the method comprising using an instruction address to fetch an instruction word; executing instructions from the fetched instruction word; detecting in which of a plurality of ranges the instruction address lies, controlling a way in which instruction execution is parallelized dependent on a detected range.

16. (Previously presented) A method according to claim 15, the method comprising adapting a width of the fetched instruction word dependent on the detected range.

17. (Previously presented) A method according to claim 15, the method comprising changing a selection of functional units of the apparatus that is used to execute the instructions dependent on the detected range.